

FIG. 1

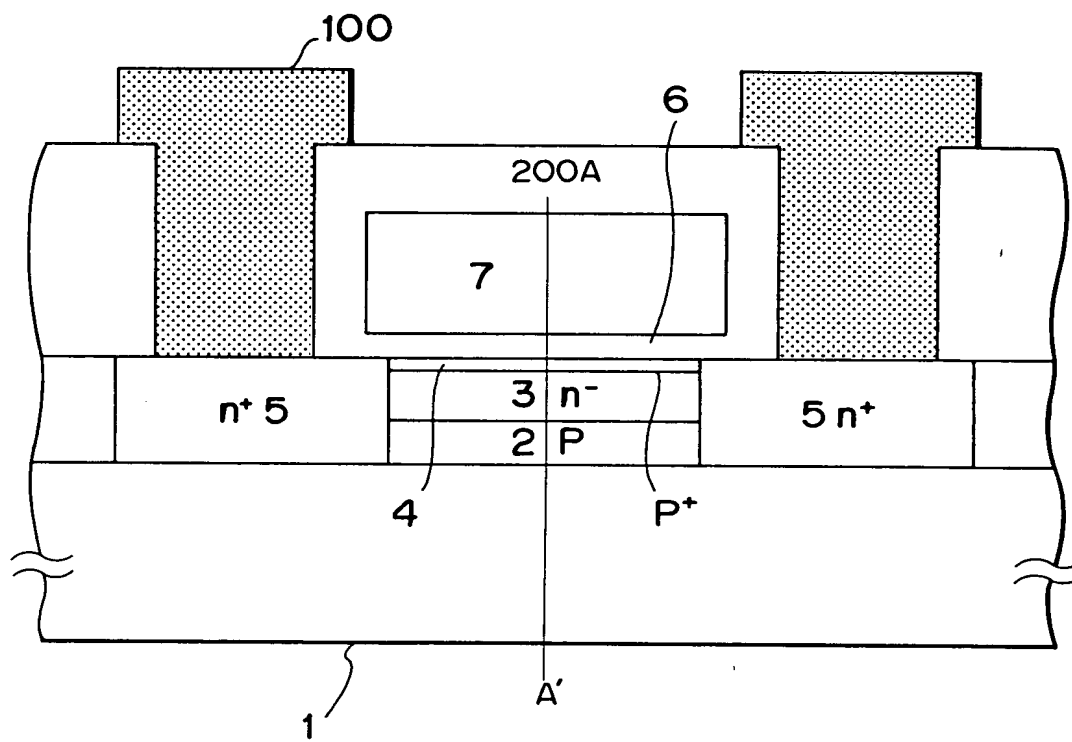
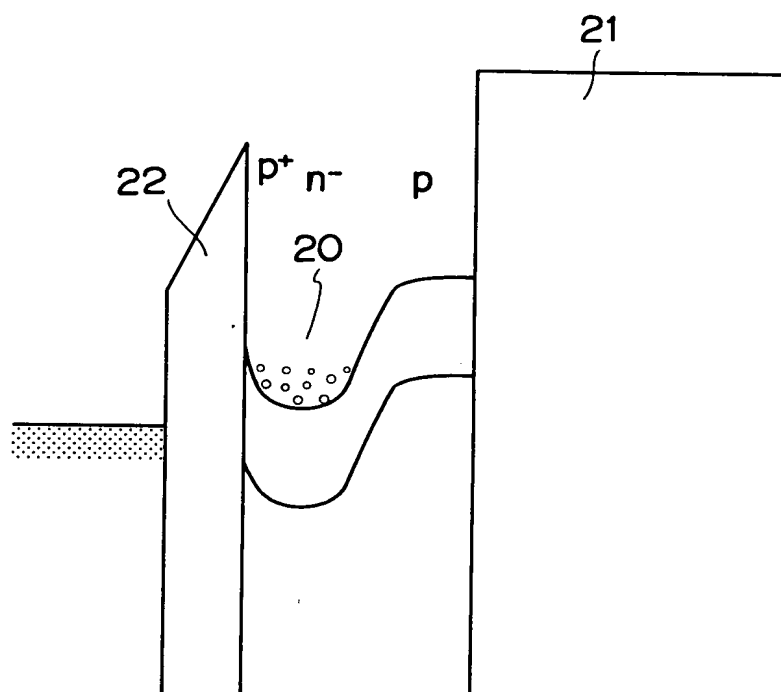


FIG. 2



# FIG. 3

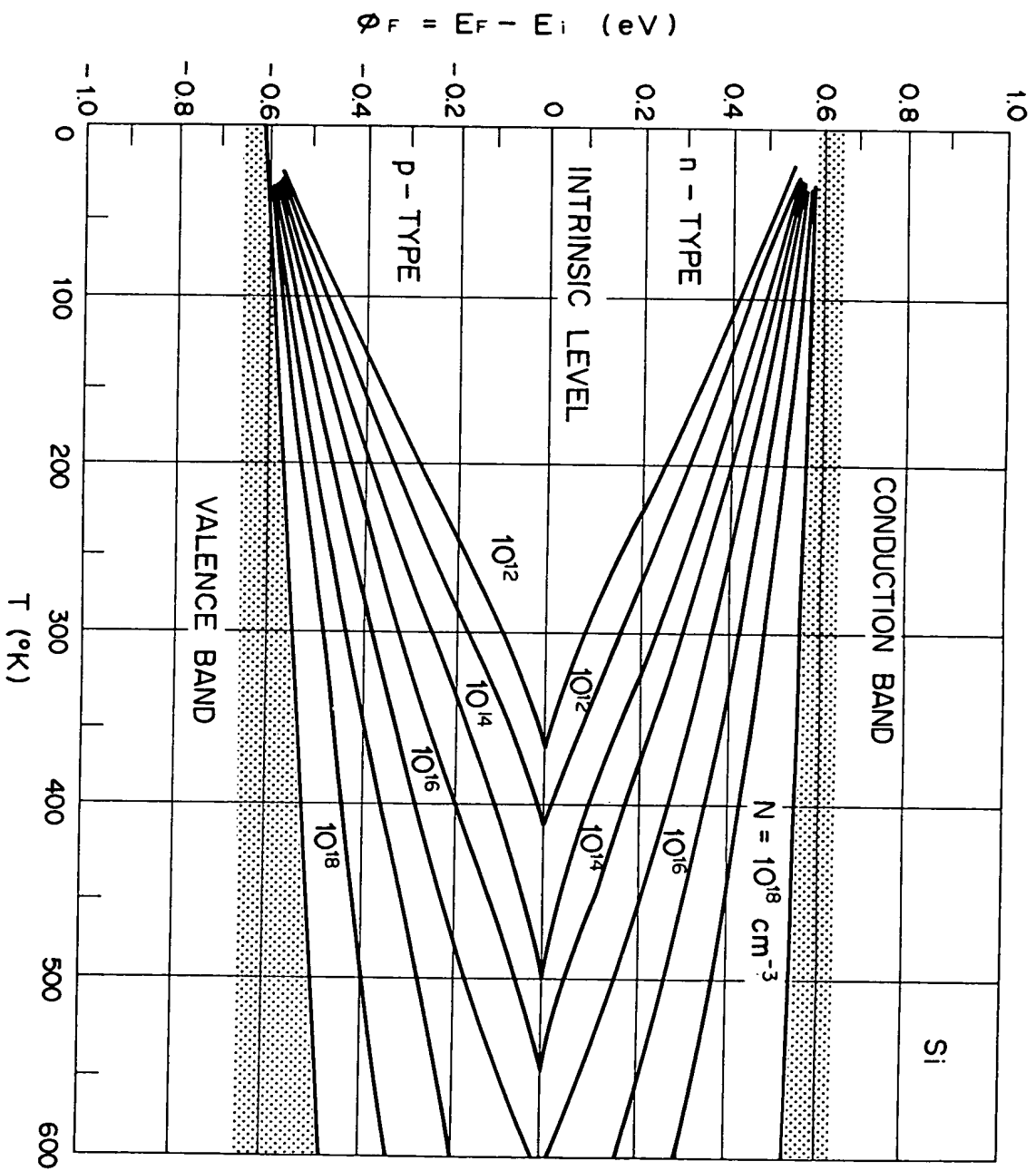


FIG. 4

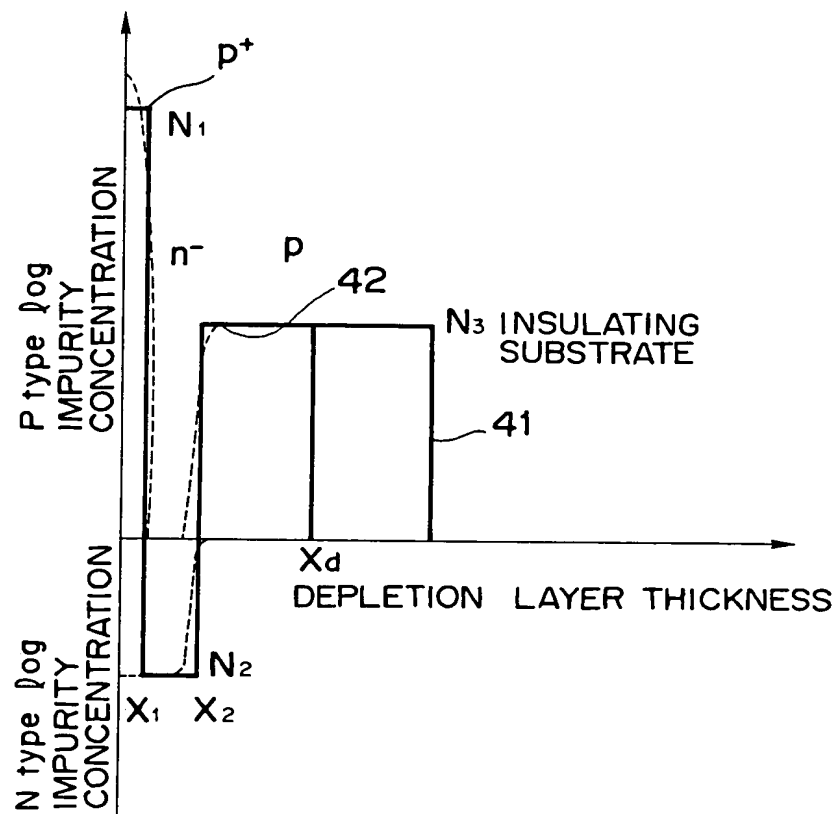


FIG. 5

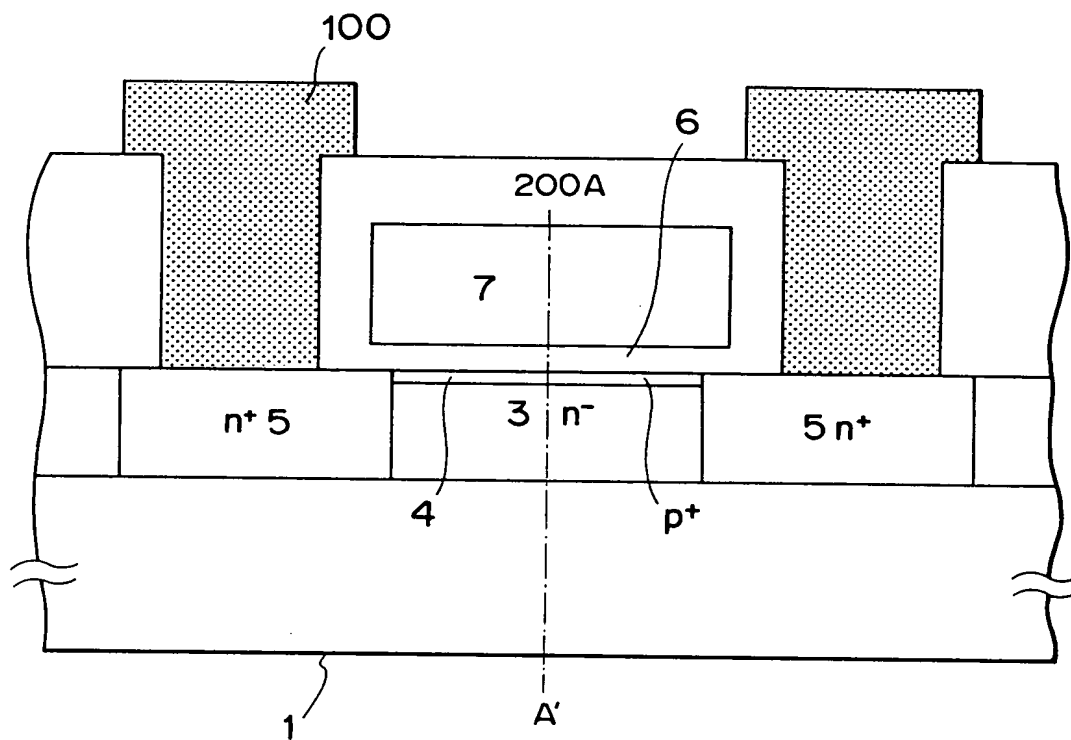


FIG. 6

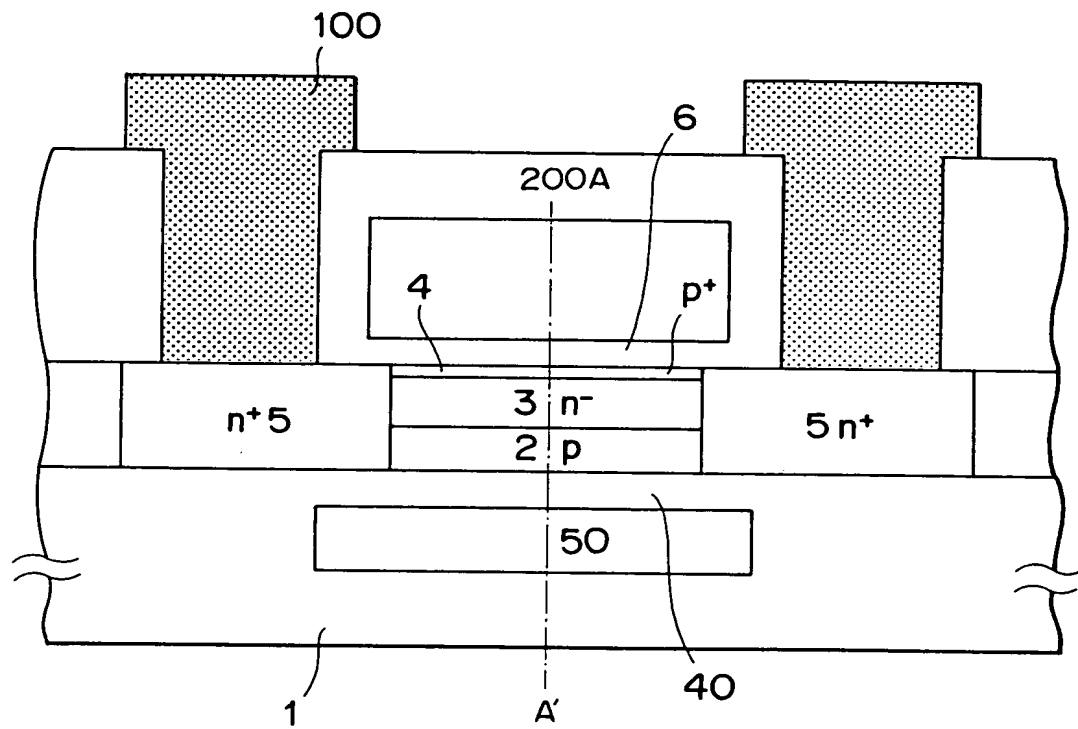


FIG. 7

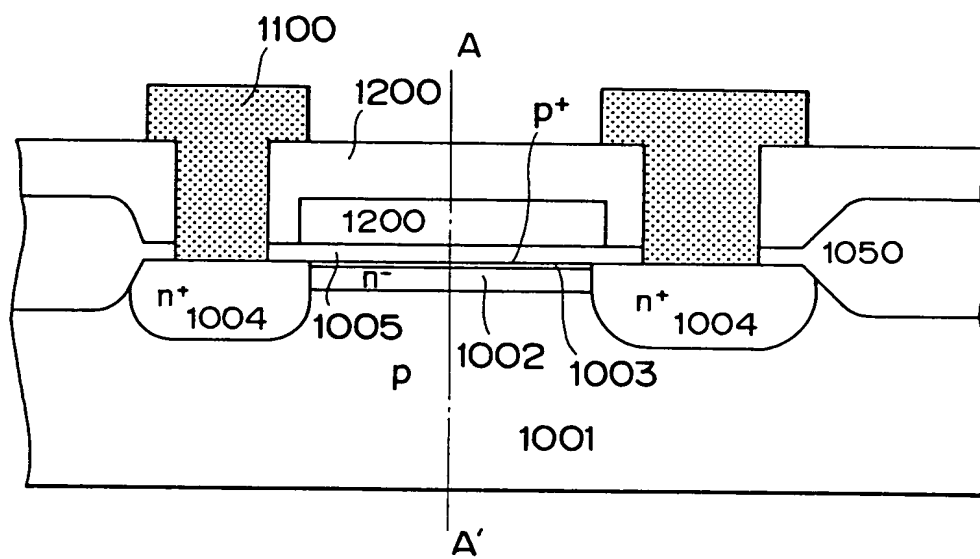


FIG. 8

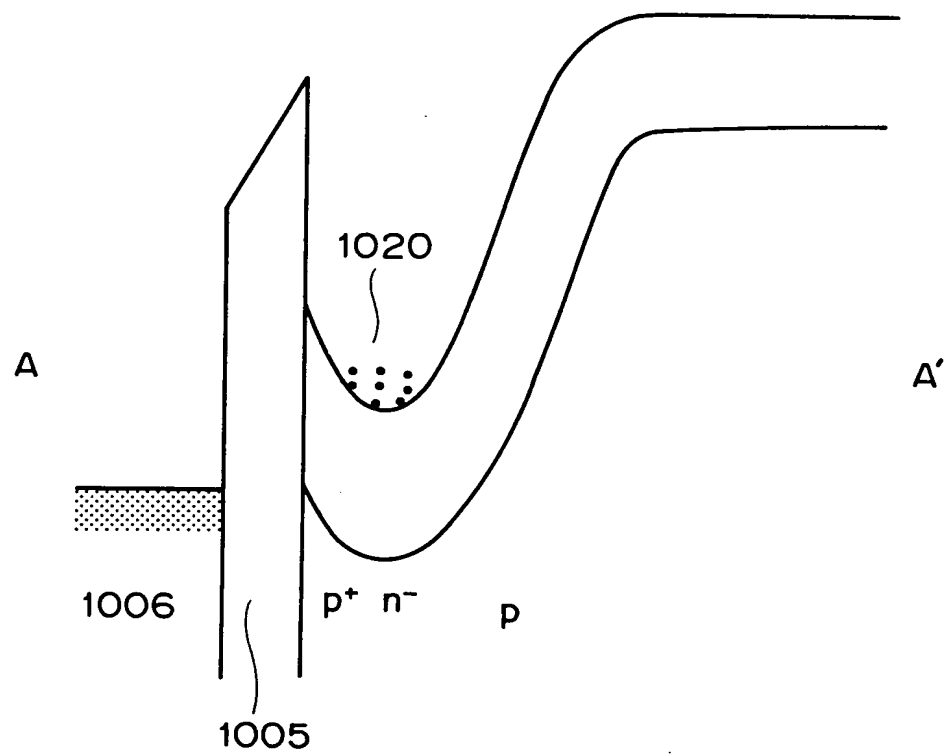




FIG. 9A

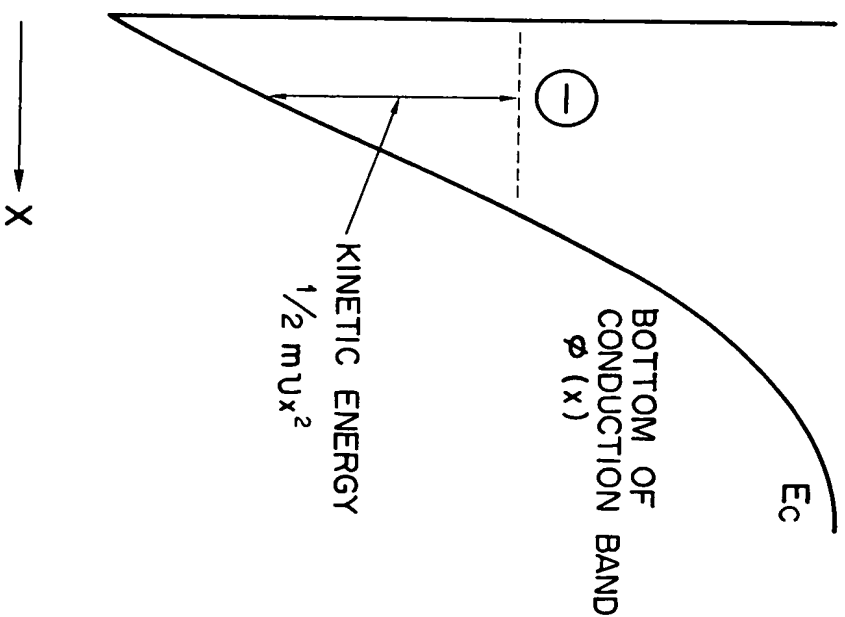
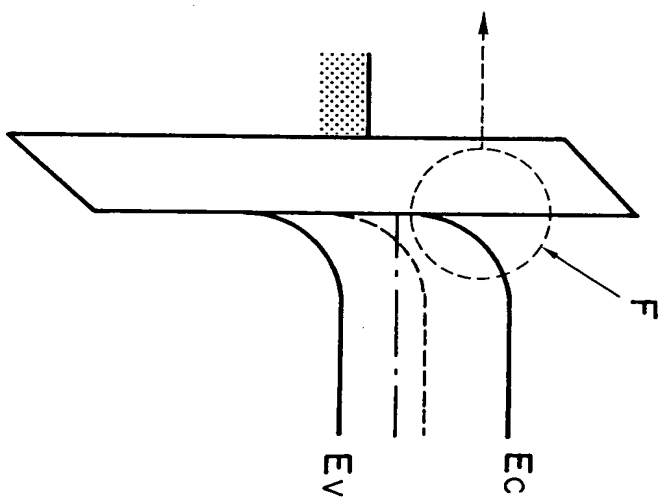


FIG. 9B



# FIG. 10

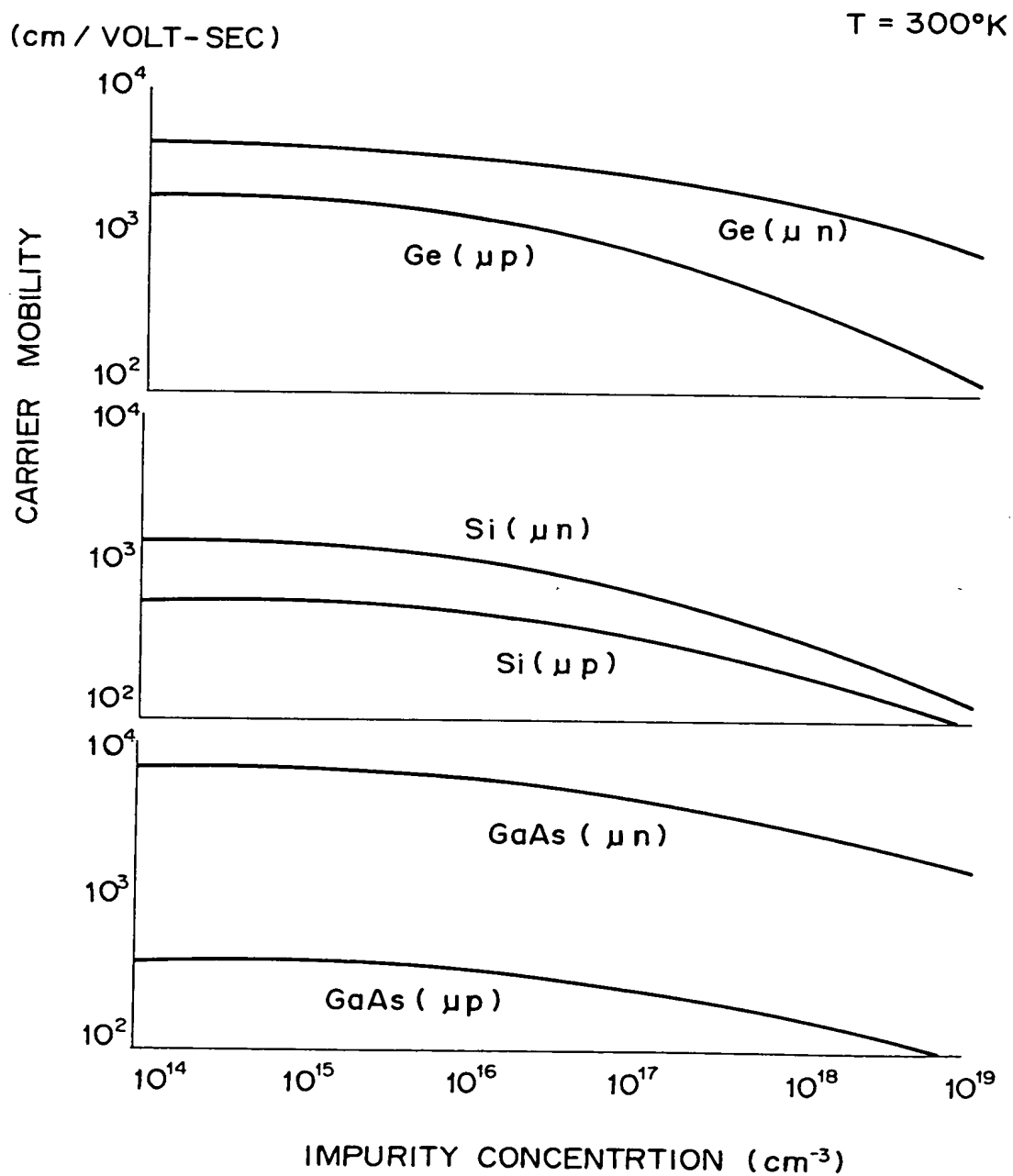
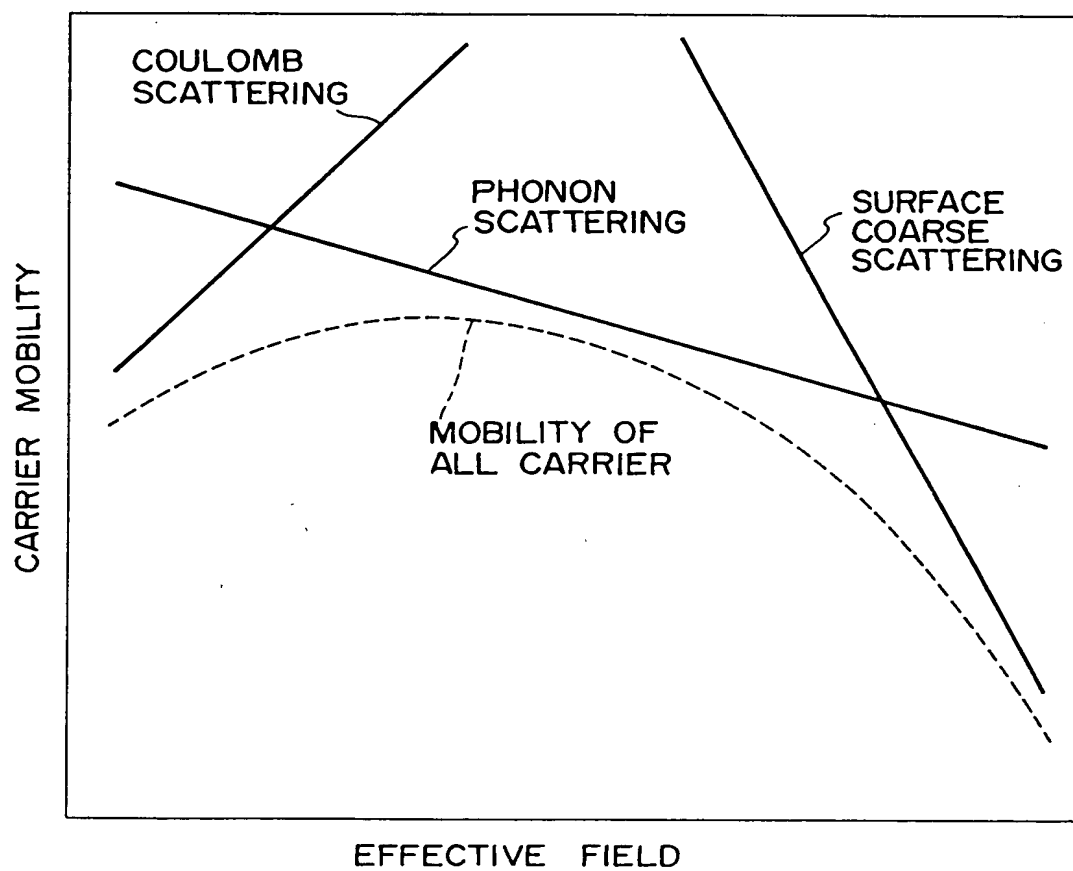


FIG. 11



F I G. 12

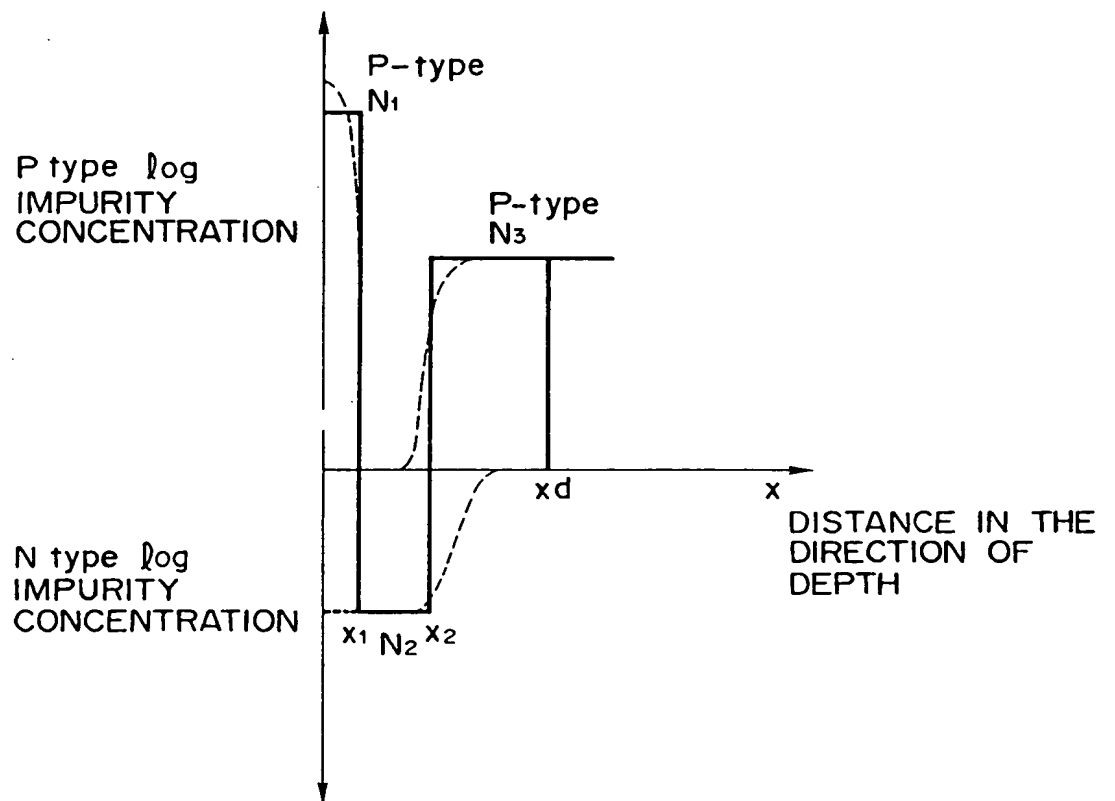
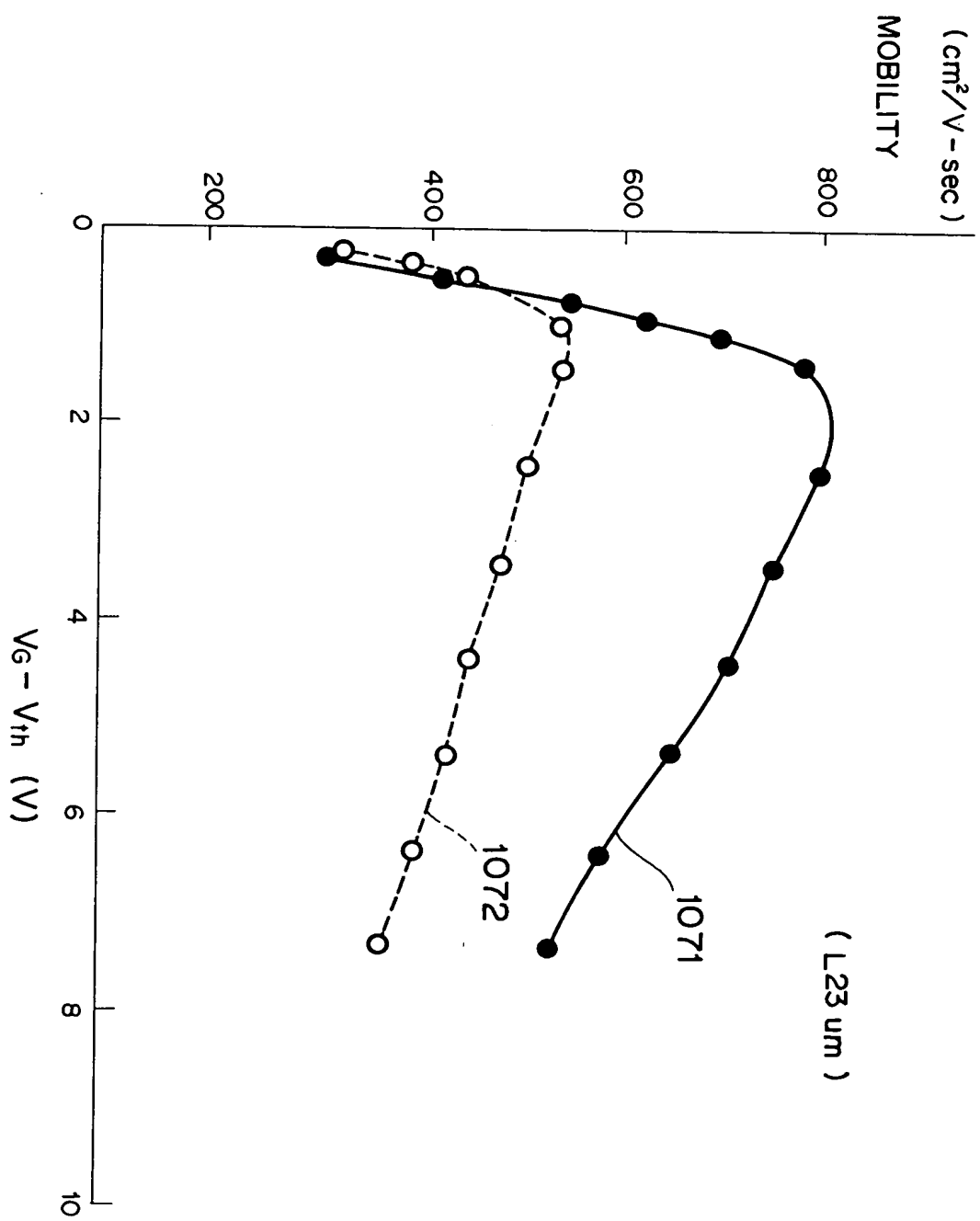


FIG. 13



A cross-sectional view of a semiconductor device 1000. The device is built on a substrate 1001, which is divided into a p-type region (labeled 'p') and an n-type region (labeled 'n'). A dashed line 'x' indicates the interface between the substrate and the device layers. The device features a central channel region 1002, which is p-type (labeled 'p+') and is flanked by n+ regions 1004 and 1003. Above the channel, there is a gate stack 1200, which includes a gate oxide 1006 and a gate electrode 1005. The gate stack is flanked by two vertical insulating regions 1100. The device is further defined by a p-type region 1050 and a p-type region P1010. The entire device is covered by a protective layer 1001.

FIG. 15

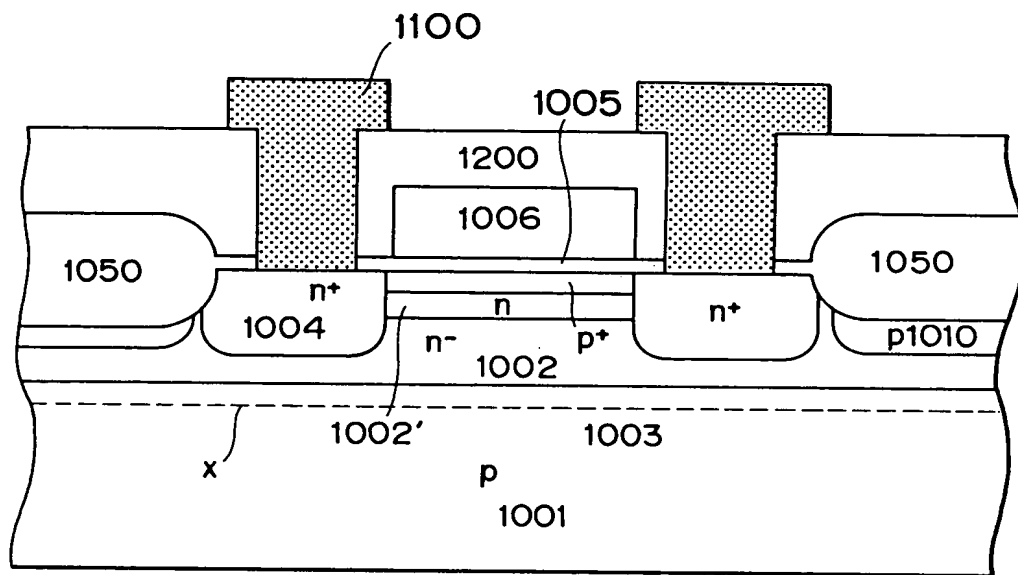


FIG. 16

